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Residual Stresses and Stacking Faults in N-Type 4H-SiC Epilayers

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Abstract. Residual stresses were measured in n-type 4H-SiC epilayers having nitrogen-doping levels of 5 x 10^{17}, 5 x 10^{18}, and 2 x 10^{19} cm^{-3} and grown homoepitaxially on n-type 4H-SiC substrates having doping levels between 1.82 and 2.10 x 10^{19} cm^{-3} (ρ = 0.010-0.011 Ω-cm). Radius of curvature measurement of the epilayer/substrate bicrystals indicates the existence of compressive stresses of magnitudes between 250 and 400 MPa. Transmission electron microscopy (TEM) examination of the epilayer/substrate bicrystals, after they were annealed at 1150°C in nitrogen for thirty minutes, revealed bands of stacking faults (SFs) confined within the epilayers that have doping levels of 5 x 10^{17} cm^{-3} and 5 x 10^{18} cm^{-3}. The SFs, some as wide as 80 nm, give rise to a 3C-SiC like stacking sequence. The lowest doping level is approximately two orders of magnitude below the threshold value of 3 x 10^{19} cm^{-3} previously proposed for the onset of SF generation in thermally annealed epilayers. The residual stress in all the epilayers was above the critical stress for dislocation formation above 1000°C in 4H-SiC, thus the partial dislocations giving rise to SFs may be stress induced and can occur across a much wider range of doping levels than previously believed.

Introduction

According to Lindefelt and coworkers, a SF in 4H-SiC acts as a one-dimensional quantum well, thus altering the physical and electronic properties of the crystal [1]. This idea is based on total energy calculations of a 4H-SiC crystal containing an intrinsic SF, where it has been found that a narrow band is split off from the bottom of the conduction band and extends about 0.2 eV into the bandgap of 4H-SiC [2]. Experimentally, we had previously reported the observation of SFs leading to formation of 3C like bands in n-type 4H-SiC epilayer doped 1.7 x 10^{19} cm^{-3} after routine oxidation or argon annealing at 1150°C [3]. Liu and coworkers proposed the formation mechanism of the SFs under such annealing conditions to be a spontaneous process where thermally generated carriers are trapped in the quantum well thus lowering the energy of the crystal [4]. Kuhr *et al.* subsequently calculated a threshold nitrogen doping level of 3 x 10^{19} cm^{-3}, below which SF generation by thermal treatment is not expected to occur [5].

A possible mechanism for the formation of *partial* (as well as *perfect*) dislocations in 4H-SiC, and thus of SFs by their motion, is stress. Surprisingly, very few efforts have been made to fully quantify the role of internal stress in the generation of SFs in SiC, and these efforts have mostly been confined to the stresses in the boules and not in the epilayers. In this work, a direct measurement of stress in SiC epilayers was performed, and the effect of thermal treatment on the epilayers was analyzed with high resolution transmission electron microscopy (HRTEM). The results of the stress measurements and the HRTEM thus allowed for a correlation between stress and the generation of SFs.

Experimental

Four commercial 2-inch diameter Si-face, (0001)-oriented, n-type single crystal 4H-SiC wafers were used for this study; three of which were off-axis (~ 8°) and the fourth was on-axis (~ 0.2°). The resistivities of the wafers were 0.010 Ω-cm (sample 1) and 0.011 Ω-cm (samples 2 and 3) for the off-axis and 0.007 Ω-cm for the on-axis (sample 4), with equivalent doping levels of 2.13, 1.82 and 3.81 x 10^{19} cm^{-3} (as determined by secondary ion mass spectroscopy), respectively. The radius of curvature, R_o, of each as-received wafer was measured with a temperature controlled film stress measurement system, which employs an optical measurement technique whereby a beam from a laser diode scans across the wafer at an angle [6]. The wafer was then gradually heated from room temperature at 2 ^{o}C/min to 500 ^{o}C as it was simultaneously scanned and the reflected beam was detected. The closeness of the wafer to the heating plate and the slow heating process helped to minimize thermal gradients and ensured uniform heating of the 2-inch wafer. The stress measurement continued as the wafer was cooled to room temperature and the new radius of curvature, R_{cool}, recorded. Subsequently, 2 μm thick epilayers with nitrogen doping levels ranging from 5 x 10^{17} to 2 x 10^{19} cm^{-3} were grown homoepitaxially (by the substrate vendor) by chemical vapor deposition (CVD) on these off-axis 4H-SiC wafers. No epilayer was grown on the on-axis wafer. Immediately after the CVD epilayer growth, another round of radius of curvature measurements, $R_{post\text{-}epi}$, was performed on the epilayer/wafer bicrystal. The wafers were annealed at 1150 ^{o}C in nitrogen for thirty minutes, then diced into 5 x 5 mm^2 squares and analyzed by HRTEM, specifically to search for the existence of SFs.

Results and Discussions

All the as-received wafers exhibited various degrees of concavity expressed in terms of radius of curvature, R_o, as shown in Table 1. This R_o was believed to correspond to the cumulative residual stress induced during boule growth, wafer sawing, and lapping and polishing. In each case, the radius of curvature after 500 ^{o}C treatment, R_{500C}, was found to increase, implying the release of some residual stress. Note that the stress relief in going from room temperature to 500 °C is more pronounced for the off-axis wafers as compared to the on-axis wafer (compare R_o and R_{500C} for the four wafers in Table 1).

Sample	R_o (m)	R_{500C} (m)	R_{cool} (m)	Epi Doping (cm^{-3})	$R_{post\text{-}epi}$ (m)	Epi Stress (MPa)	R_{1500C} (est.) (m)	Epi Stress (est.) (MPa)
1	13.2	15.6	15.6	2 x 10^{19}	32.5	-251	23.7	-85.6
2	38.6	58.4	76.7	5 x 10^{18}	-24.4	-406.1	150.9	-357.9
3	18.6	22.1	23.6	5 x 10^{17}	-122.9	-376.1	36.2	-267.0
4	6.9	7.7	6.4	N/A	N/A	N/A	11.7	N/A

Table 1: Changes in wafer radius of curvature before epilayer growth, R_o, and in the epilayer/wafer bicrystal after growth, $R_{post\text{-}epi}$, and the corresponding calculated stress. Epi Stress(est) is the epilayer stress calculated based on the extrapolation of the substrate radius of curvature, R_{1500C}, before typical epilayer growth at 1500 ^{o}C.

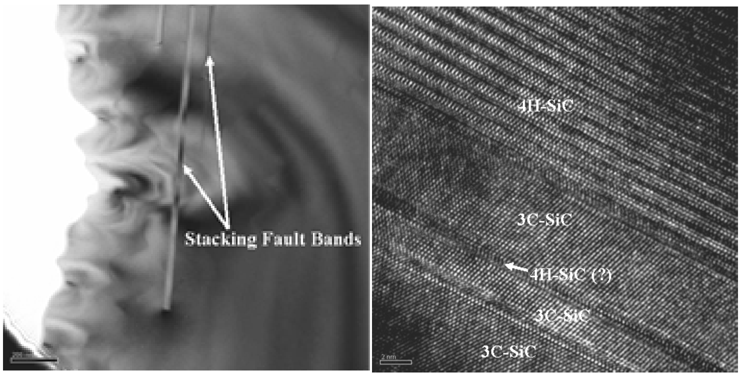
This is consistent with measurements on other on-axis n-type 4H-SiC wafers [7], indicating that thermal deformation of the on-axis wafer is less than the off-axis ones, possibly because of the lower Schmid factor in the former. The R_{cool} showed little change from R_{500C}, indicating that the relaxation was irreversible and that the relieved stress at 500 °C was via thermoplastic deformation (The R_{cool} value of sample 2 was tentatively considered an outlier since no reason is currently known for this behavior). However, the radius of curvature of the epilayer/substrate bicrystal immediately after epilayer CVD growth, $R_{post\text{-}epi}$, showed a significant increase. From the radius of curvature measurements, $R_{post\text{-}epi}$, the biaxial stress in the epilayer can be calculated from Stoney's equation, expressed as [8]:

$$\sigma_f = E_s d_s^{\,2} \left[6(1-\nu)Rt_f\right]^{-1}$$

(1) where E_s, d_s, and ν are the substrate Young's modulus (Pa), thickness (m), and Poisson's ratio, respectively; t_f is the film thickness (m), and $1/R$ = ($1/R_{post\text{-}epi}$ - $1/R_{cool}$) (m^{-1}). The results shown in Table 1 indicate that the biaxial stresses in the post growth epilayers are compressive with estimated magnitudes between 250 MPa and 410 MPa. However, extrapolation of the radius of curvature to the typical growth temperature of 1500 ^{o}C for 4H-SiC epilayers [9] resulted in stress magnitudes estimated between 80 and 270 MPa (see Table 1). By resolving the bi-axial stress to the

8° tilted basal (0001) plane and along the $\langle 11\bar{2}0 \rangle$ direction, shear stresses that are greater than those required to generate dislocations in 4H-SiC [10, 11] are obtained.

TEM examination of all four epilayer/substrate bicrystal after annealing at 1150 ^{o}C revealed SF bands exclusively in the epilayers of samples with doping levels of 5 x 10^{17}, as shown in Fig. 1. Fig. 1b is a HRTEM of one of the bands, indicating the occurrence of multiple faults that lead to moderately thick layers with a 3C stacking sequence. SFs were also observed in the epilayer with a doping level of 5 x 10^{18} cm^{-3} as shown in the TEM image in Fig. 2. These doping levels are one and two orders of magnitude below the threshold value proposed in [5] for the formation of double



(a) *(b)*

Fig. 1: The cross section TEM images of off-axis n-type 4H-SiC substrate with 5 x 10^{17} cm^{-3}, 2 µm epilayer annealed at 1150°C in nitrogen ambient for 30 minutes showing a) three SF bands, and b) HRTEM of one of the bands showing sub-bands of 4H-SiC that transformed to 3C-SiC stacking sequence.

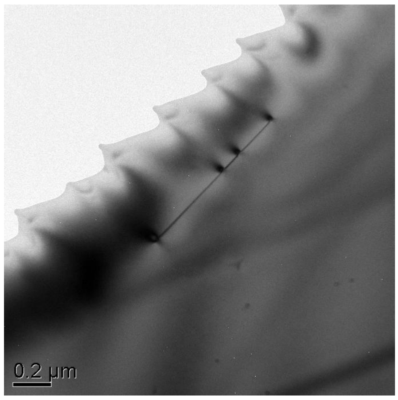


Fig. 2: TEM image of a SF in the 2 µm thick 4H-SiC epilayer having doping level of 5 x 10^{18} cm-3 and grown on substrate with a doping level of 1.8 x 10^{19} cm^{-3}.

faults. No SF bands were observed in the 2 x 10^{19} cm^{-3} epilayer, although we had previously observed SFs in epilayer with 1.7 x 10^{19} cm^{-3} concentration [3]. The existence of these SFs in annealed 4H-SiC of such low doping levels cannot be explained with the quantum well action (QWA) model because in these two cases, the Fermi level should lie several tenth eV below the E_c - 0.2 eV position of the split-off band [2]. Thus, the observation of SFs in samples with doping levels much lower than the proposed threshold of 3 x 10^{19} cm^{-3} appears to limit the validity of QWA to doping levels greater than 3 x 10^{19} cm^{-3}. Also significant is that the characteristic SF features were not observed in the highly doped (3.81 x 10^{19} cm^{-3}) *on-axis* 4H-SiC substrate even after annealing it at 1150°C, an observation very different from the annealed *off-axis* highly doped 4H-SiC substrate [12] . By applying the QWA model to highly doped wafers, SFs should be generated in this thermally treated on-axis wafers, just as in off-axis, unless SFs do not occur in on-axis substrates as readily as they do in the off-axis cut wafers. One could presume that at temperatures above ~1000 °C, the residual shear stress induces the formation of either perfect (albeit widely dissociated into two partials) or single leading partials in the crystal. The dislocations can nucleate at heterogeneities at the wafer surface (e.g. scratches) or within the crystal (dislocations). The observation of stacking faults is evidence for the formation of the leading partial, rather than perfect, dislocations. If there is no electronic mechanism involved, however, the motion of these partial dislocations to generate stacking faults requires the presence of a sufficiently high shear stress in the crystal. In our measurements, the residual stresses in the epilayers were above the estimated critical stress for both dislocation formation [10, 11] and dislocation motion at the annealing temperature.

Conclusions

This work allows us to present the following conclusions: Thermally generated SFs would likely occur only if nucleation sites for partial dislocations exist in the crystal. Irrespective of the doping level, the residual stress in commercially grown 4H-SiC epilayers is large enough to nucleate and initiate the motion of partial dislocations at temperatures above 1000 °C. The QWA model does not explain the generation of SFs that were observed in epilayers having doping levels far below 3 x 10^{19} cm^{-3}. Large compressive stresses in as grown 4H-SiC epilayers exist and because of the tilt of the basal planes in commercial SiC wafers, these compressive stresses can give rise to significant shear stresses. Thus, it is possible that the stacking fault bands observed in many recent experiments are caused by the generation of leading partial dislocations induced by residual stresses in the 4H-SiC layer. In contrast to highly n-doped *off-axis* 4H-SiC wafers, annealing of an *on-axis* 4H-SiC wafer with similar high doping levels does not appear to result in the formation of stacking faults. However, a more extensive study in this regard is required.

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